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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,732	05/27/2005	Eric Desmicht	FR02 0129 US	4315

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EXAMINER	
OKEKE, IZUNNA	

ART UNIT	PAPER NUMBER
2432	

NOTIFICATION DATE	DELIVERY MODE
03/25/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/536,732	DESMICHT ET AL.	
	Examiner	Art Unit	
	IZUNNA OKEKE	2432	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 01/05/2010, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Gilberto Barron Jr./
Supervisory Patent Examiner, Art Unit 2432

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3, 5-13 have been considered and are persuasive. However, updating the search resulted in a discovery of new prior art neccessitating new ground(s) of rejection. The delay in citation of the newly discovered prior art is regretted.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 5, 7-8, 9, and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakaki et al. (US-5826007).

a. *Referring to claim 1, 9 and 11:*

Regarding claim 1, Sakaki teaches a chip for processing a content, comprising at least a microprocessor, characterized in that said chip includes an integrated non-volatile programmable memory for storing for storing protection data and protected data (Col 4, Line 13-48..... chip comprising CPU, protected test memory (storing a test program) and protection bits (S1, S2) for protecting access to the protected memory), said protection data being intended to define a protection level for authorizing/denying access to said protected data by said microprocessor while a program is executed (Col 4, Line 42 thru Col 5, Line 48.... The protection bits (s1, S2) define a protection level for the protected data in that access (Read/write) to the data is authorized when the bits are in their low level (logic 0) and denied when s1 is changed to a high level (logic 1)), wherein said protection data is only modifiable so as to increase the said .protection level (Col 2, Line 36-41 Col 5, Line 44-46.... Protection bit s1 is modified to high level (logic 1) to increase the protection level from the initial state and deny access to the stored test program) and said protected data includes data to activate/deactivate an optional feature of the chip (Col 4, Line 28-30 and Col 5, Line 34-42.... protected test program used to enable/disable read/write (input/output) to the NV memory from an external terminal).

a. *Referring to claim 3:*

Regarding claim 3, Sakaki teaches a chip according to Claim 1, wherein said protection data includes a password, said access being authorized/denied through a password check (Col 5, Line 13 thru Col 6, Line 12….. s1 and s2 protection bits with s2 comprising the password check. If s1=1, the chip is password-protected and access to the protected data is denied. If s1=1 and s2=1 (s2 being the password check), a manufacturer can then access the protected data after shipment).

a. *Referring to claim 5:*

Regarding claim 5, Sakaki teaches a chip according to Claim 1, wherein said optional feature is a connection to an external device for downloading a program and/or data from said external device (Col 5, Line 34-43…. connection to an external terminal for inputting or outputting data into the memory of the chip).

a. *Referring to claim 7:*

Regarding claim 7, Sakaki teaches a chip according to Claim 1, wherein said protection data includes a value defining an address limit from which the data stored at said memory are protected data and access to such protected data is denied (Col 6, Line 3-16…. Based on the value of the s1, s2 protection bits, the bus control logic defines the address of the protected data which the CPU can execute).

a. *Referring to claim 8:*

Regarding claim 8, Sakaki teaches a chip according to Claim 7, wherein said protected data include includes programs and data operating a conditional-access dedicated microprocessor (Col 4, Line 13-35…. protected memory storing system program and fixed data for operating a microprocessor) .

a. *Referring to claim 12:*

Regarding claim 12, Sakaki teaches a chip according to Claim 1 further comprising a random logic coupled between said integrated non-volatile programmable memory and a connection bus of said microprocessor (Fig 2. bus line control circuit coupled between the protected memory and the processor).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki et al. (US-5826007), and further in view of Madter et al. (US-20050033951).

a. *Referring to claim 6:*

Regarding claim 6, Sakaki teaches the protected data includes data to activate/deactivate and external feature of the microprocessor such as write/read to an external terminal. Sakaki does not teach external feature of downloading a boot program from an external memory. However, the concept of protecting a chip from downloading an external boot program (which might be malicious) using protection bits is well known in the art. For instance, Madter discloses an on-chip security method wherein a security value (protection data) is used to protect flash memory. The password is used to protect access to instructions for downloading an external boot program to be run by the chip. When a password is received (password check), download of the external boot program is inhibited (See Sakaki, Para 32-35). Therefore, it would have been obvious to

modify Sakaki's protection system to include protection against downloaded boot programs wherein the protection bits of Sakaki are used to enable or disable access to external boot programs for the purpose of securing the chip from both unauthorized and malicious access.

a. *Referring to claim 10:*

Regarding claim 10, Sakaki teaches a device as claimed in Claim 9, wherein the device is intended to process encrypted video/audio data (See Madter, Para 3… PDA and mobile devices for processing encrypted video/audio as known in the art).

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki et al. (US-5826007) and Madter et al. (US-20050033951), and further in view of Boyle et al. (US-6118870).

a. *Referring to claim 13:*

Regarding claim 13, Sakaki teaches a chip according to claim 1. Sakaki does not explicitly teach the chip having a MIPS instruction set. However, Boyle teaches a chip having a MIPS instruction set (See Boyle, Col 10, Line 3-18). Therefore it would have been obvious to one of ordinary skill to implement Sakaki's chip as a microprocessor having a MIPS instruction set for the benefit of utilizing RISC architecture which provides higher performance by making instruction execute quickly and is designed for use with high level programming languages.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IZUNNA OKEKE whose telephone number is (571)270-3854. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571) 272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/IZUNNA OKEKE/
Examiner, Art Unit 2432

/Gilberto Barron Jr./
Supervisory Patent Examiner, Art Unit 2432